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EXAMINER	
VITAL, PIERRE M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 12/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,800	NEUMAN, PAUL S.	
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed September 30, 2003 in response to PTO Office Action mailed June 27, 2003. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. Claims 1-20 have been presented for examination in this application. In response to the last Office Action, claims 1 and 6 have been amended. No claims have been canceled. No claims have been added. As a result, claims 1-20 are now pending in this application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 11 and 16 is rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (US6,397,300).

As per claim 11, Arimilli discloses a method of maintaining validity of data within a level one cache memory of a processor responsively coupled to a level two cache memory

which is responsively coupled to a system memory bus [*L1 cache 200, L2 cache 202, system bus 105*; Fig. 4] comprising: formulating a write request [*issuing store operation*; col. 12, lines 10]; first experiencing a level one cache memory miss in response to said write memory request [col. 12, line 18]; second experiencing a level two cache memory hit in response to said first experiencing step [col. 9, lines 33-34, col. 12, lines 54-56]; and invalidating a portion of said level one cache memory corresponding to said write memory request in response to said second experiencing step [*cache line in an upper level cache invalidated when a store operation is passed to a lower level cache and the store hits in the upper level cache*; col. 5, lines 12-25].

As per claim 16, Arimilli discloses an apparatus comprising means for executing program instructions [*processor 122*; Fig. 2]; means responsively coupled to said executing means for level one caching data [*L1 cache 200*; Fig. 4]; means responsively coupled to said executing means and said level one caching means for accessing a data element if said executing means requires accessing of said data element and said level one caching means does not contain said data element [*controller 14 responding to L1 cache misses; system memory coupled to system bus 105*; col. 9,, lines 33-44; Fig. 4]; means responsively coupled to said requesting means for level two caching data [*L2 cache 202*; Fig. 4]; and means responsively coupled to said level one caching means for invalidating said data element if said data element is a write data element located within said level two caching means [*cache line in an upper level cache invalidated when a store*

operation is passed to a lower level cache and the store hits in the upper level cache; col. 5, lines 12-25].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pong et al. (US6,253,291) and Lynch et al. (US6,061,766).

As per claim 1, Pong discloses a data processing system having a system bus and having a processor [*system bus 18; processors 22, 42, 62, 82, 102, 132*; Figs. 2-7], with a level one cache memory [*L1 caches 32, 52, 74, 92, 114, 138*; Figs. 2-7], responsively coupled to a level two cache memory [*L2 caches 34, 54, 72, 94, 112, 140*; Figs. 2-7], which is responsively coupled to a level three cache memory which is directly coupled to at least one memory storage [*L3 caches 28, 68, 88, 108 inherently coupled to main memory through system bus 18*; Figs. 2-7]; and having a circuit for Snooping said system bus [*snoop queues 24, 44, 64, 84, 104*; Figs. 2-7].

However, Pong does not specifically teach first logic which invalidates a corresponding level one cache memory location in response to either a non-local write or write ownership request as recited in the claim.

Lynch discloses first logic which invalidates a corresponding level one cache memory location in response to either a non-local write or write ownership request [*processor invalidate data in their own memories (or on-chip caches) when request for exclusive use is granted;* col. 1, lines 40-48, 53-55; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*].

As per claim 2, Pong does not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership as recited in the claim.

Lynch further discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership [*snoop requests checks for the presence of an object in cache; only requests for exclusive use which match cache tags are invalidated; there is no invalidate is done when there is no hit*; Fig. 4; col. 4, lines 19-30; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*].

As per claim 3, Pong does not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit as recited in the claim.

Lynch discloses third logic which invalidates said corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*].

It would have been obvious to one of ordinary skill in the art, having the teachings of Pong and Lynch before him at the time the invention was made, to modify the system of Pong to include first logic which invalidates a corresponding level one cache memory location in response to either a non-local write or write ownership request; a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership; and third logic which invalidates said corresponding cache memory location in response to a SNOOP hit because it would have (1) maintained coherence among multiple copies of an object by insuring that for every valid write to one copy of an object, the system must update or invalidate every other copy of the object [col. 1, lines 18-20]; and (2) provided a snoop process for ensuring cache coherency and an increase in the hit rate of the system as taught by Lynch by invalidating a data object a data object contained in the on-chip cache and checking for the presence of the data object in the on-chip cache [col. 2, lines 20-21, 34, 60-65] as taught by Lynch.

7. Claims 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pong et al. (US6,253,291) and Lynch et al. (US6,061,766) and Mounes-Toussi et al. (US6,425,060).

As per claim 4, the combination of Pong and Lynch discloses the claimed invention as detailed above in the previous paragraphs. However, Pong and Lynch do not specifically teach fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read.

Mounes-Toussi discloses fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read [col. 8, lines 44-61; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*].

It would have been obvious to one of ordinary skill in the art, having the teachings of Pong and Lynch and Mounes-Toussi before him at the time the invention was made, to modify the system of Pong and Lynch to include fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read because it would have provided a data processing system which maintains coherence by using a multi-level coherence mechanism that relies on appropriate requests and replies transferred between the various memories in a shared memory system [col. 8, lines 36-41] as taught by Mounes-Toussi.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pong et al. (US6,253,291) and Lynch et al. (US6,061,766) and Hazawa (US4,891,809).

As per claim 5, the combination of Pong and Lynch discloses the claimed invention as detailed above in the previous paragraphs. However, Pong and Lynch do not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col.3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Pong and Lynch and Hazawa before him at the time the invention was made, to modify the system of Pong and Lynch to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pong et al. (US6,253,291) and Arimilli et al. (US6,397,300).

As per claim 6, Pong discloses a data processing system comprising a level one cache memory [*L1 caches 32, 52, 74, 92, 114, 138*; Figs. 2-7]; a level two cache memory responsively coupled to said level one cache memory [*L2 caches 34, 54, 72, 94, 112, 140*; Figs. 2-7]; a system bus [*system bus 18*; Figs. 2-7]; a memory storage unit [*main memory*; col. 4, lines 19-22]; a level three memory responsively coupled to said level two cache memory via said system bus and responsively coupled to said memory storage unit [*L3 caches 28, 68, 88, 108 inherently coupled to main memory through system bus 18*; Figs. 2-7].

However, Pong does not specifically teach a first circuit to invalidate a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write as recited in the claim.

Arimilli discloses a first circuit to invalidate a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write [*cache line in an upper level cache invalidated when a store operation is passed to a lower level cache and the store hits in the upper level cache*; col. 5, lines 12-25].

It would have been obvious to one of ordinary skill in the art, having the teachings of Pong and Arimilli before him at the time the invention was made, to modify the system of Pong to include a first circuit to invalidate a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write because it would have improved the operation of the caches

by forwarding all stores down to the lower level cache [col. 5, lines 40-46] as taught by Arimilli.

10. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pong et al. (US6,253,291) and Arimilli et al. (US6,397,300) and Lynch et al. (US6,061,766).

As per claim 7, the combination of Pong and Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Pong and Arimilli do not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership.

Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership [*snoop requests checks for the presence of an object in cache; only requests for exclusive use which match cache tags are invalidated*; *there is no invalidate is done when there is no hit*; Fig. 4; col. 3, line 56 – col. 4, line 30; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow*; *clearly, the use of multiple logics is an inherent feature of any computer system*].

As per claim 8, the combination of Pong and Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Pong and Arimilli do not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit.

Lynch discloses third logic which invalidates said corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*].

It would have been obvious to one of ordinary skill in the art, having the teachings of Pong and Arimilli and Lynch before him at the time the invention was made, to modify the system of Pong and Arimilli to include a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership, logic which invalidates said corresponding cache memory location in response to a SNOOP hit, because it would have (1) maintained coherence among multiple copies of an object by insuring that for every valid write to one copy of an object, the system must update or invalidate every other copy of the object [col. 1, lines 18-20]; and (2) provided a snoop process for ensuring cache coherency and an increase in the hit rate of the system as taught by Lynch by invalidating a data object a data object contained in the on-chip cache and checking for the presence of the data object in the on-chip cache [col. 2, lines 20-21, 34, 60-65] as taught by Lynch.

11. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pong et al. (US6,253,291) and Arimilli et al. (US6,397,300) and Mounes-Toussi et al. (US6,425,060).

As per claim 9, the combination of Pong and Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Pong and Arimilli do not specifically teach fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss.

Mounes-Toussi discloses fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss [col. 8, lines 44-61; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*].

It would have been obvious to one of ordinary skill in the art, having the teachings of Pong and Arimilli and Mounes-Toussi before him at the time the invention was made, to modify the system of Pong and Arimilli to include fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read because it would have provided a data processing system which maintains coherence by using a multi-level coherence mechanism that relies on appropriate requests and replies transferred between the various memories in a shared memory system [col. 8, lines 36-41] as taught by Mounes-Toussi.

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pong et al. (US6,253,291) and Arimilli et al. (US6,397,300) and Hazawa (US4,891,809).

As per claim 10, the combination of Pong and Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Pong and Arimilli do not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col. 3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Pong and Arimilli and Hazawa before him at the time the invention was made, to modify the system of Pong and Arimilli to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

13. Claims 12-13 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Lynch et al. (US6,061,766).

As per claims 12 and 17, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership.

Lynch discloses a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership [*snoop requests checks for the presence of an object in cache; only requests for exclusive use which match cache tags are invalidated*; *there is no invalidate is done when there is no hit*; Fig. 4; col. 3, line 56 – col. 4, line 30; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow*; *clearly, the use of multiple logics is an inherent feature of any computer system*].

As per claims 13 and 18, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli do not specifically teach third logic which invalidates said corresponding cache memory location in response to a SNOOP hit.

Lynch discloses third logic which invalidates said corresponding cache memory location in response to a SNOOP hit [Fig. 4; col. 4, lines 24-26; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow*; *clearly, the use of multiple logics is an inherent feature of any computer system*].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Lynch before him at the time the invention was made, to modify the system of Arimilli to include a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership, logic which invalidates said corresponding cache memory location in response to a SNOOP hit, because it would have (1) maintained coherence among multiple copies of an object by insuring that for every valid write to one copy of an object, the system must update or invalidate every other copy of the object [col. 1, lines 18-20] as taught by Lynch; and (2) provided a snoop process for ensuring cache coherency and an increase in the hit rate of the system by invalidating a data object a data object contained in the on-chip cache and checking for the presence of the data object in the on-chip cache [col. 2, lines 20-21, 34, 60-65] as taught by Lynch.

14. Claims 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Mounes-Toussi et al. (US6,425,060).

As per claims 14 and 19, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss.

Mounes-Toussi discloses fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read miss [col. 8, lines 44-61; *it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is designed to follow; clearly, the use of multiple logics is an inherent feature of any computer system*].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Mounes-Toussi before him at the time the invention was made, to modify the system of Arimilli to include fourth logic which retrieves and records data in response to a level one cache read miss and a level two cache memory read because it would have provided a data processing system which maintains coherence by using a multi-level coherence mechanism that relies on appropriate requests and replies transferred between the various memories in a shared memory system [col. 8, lines 36-41] as taught by Mounes-Toussi.

15. Claims 15 and 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (US6,397,300) and Hazawa (US4,891,809).

As per claims 15 and 20, Arimilli discloses the claimed invention as detailed above in the previous paragraphs. However, Arimilli does not specifically teach invalidating a level one cache memory in response to a level two cache memory generating a parity error as recited in the claim.

Hazawa discloses invalidating a level one cache memory in response to a level two cache memory generating a parity error [col. 3, lines 38-48].

It would have been obvious to one of ordinary skill in the art, having the teachings of Arimilli and Hazawa before him at the time the invention was made, to modify the system of Arimilli to include invalidating a level one cache memory in response to a level two cache memory generating a parity error because it would have provided a cache memory having a normal error checking mode as taught by Hazawa by the provision of a sequential verification logic circuit for generating error indicating signals in sequence within the cache memory unit [col. 1, lines 30-37] as taught y Hazawa.

Response to Arguments

16. Applicant's arguments with respect to claims 1, 6 and 16 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed September 30, 2003 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

(a) Lynch does not teach second logic which inhibits which said first logic from invalidating for mode 3 requests without ownership.

Examiner respectfully traverses for the following reasons. A "mode 3 write without ownership" as described in the specification means "there is no data within the level one operand cache memory to invalidate". Examiner would like to point out that Lynch teaches that when a processor desires exclusive use (i.e., ownership) of an object, a *snoop is applied to the bus and checks for the presence of an object in cache. Requests matching the snoop address (i.e., requests for exclusive use) and cache tags are invalidated* as detailed in col. 3, line 56 – col. 4, lines 19-30. As can be clearly seen in Fig. 4, the system does not invalidate when there is no hit (i.e., no data to invalidate) (steps 412 - 420).

(b) The prior art does not teach second logic, third logic, fourth logic, etc..

Examiner respectfully traverses for the following reasons. As detailed in the response mailed June 27, 2003 (Paper No.7), it is clearly obvious that any computer system uses a combination of logic to produce output based on the rules of logic it is

designed to follow. Thus, multiple logics must be used as part of the system to obtain desired results. Clearly, the use of multiple logics is an inherent feature of any computer system.

(c) Arimilli does not have any cache snoop tags and cannot be combined with Lynch.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Arimilli and Lynch deal with cache invalidation and snooping. Even though Arimilli is silent about cache tags, the use of tags in cache for comparison in cache data access in inherent to the Arimilli reference and is well known in the state of the art and does not constitute the novelty of applicant's invention.

(d) Mounes-Toussi does not disclose the "recording" in any form.

Examiner respectfully traverses for the following reasons. Note that in column 8, lines 62-65, Mounes-Toussi discloses that the data is placed in the L1 and L2 caches. Thus, it can be clearly seen that data is recorded in the caches after it is retrieved.

Conclusion

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111 (c) to consider these references fully when responding to this action. The documents cited therein teach retrieving and recording data in response to L1 and L2 cache misses.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

Pierre M. Vital
Art Unit 2188
December 1, 2003